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VS-2510 All-In-One Low Power PC/104 Geode CPU Board User's Manual

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- ❑ Description of you peripheral attachments
- ❑ Description of your software (operating system, version, application software, etc.) and BIOS configuration
- ❑ Description of the symptoms (Extract wording any message)

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Chapter 1 Introducing the VS-2510 System Board

Overview

The VS-2510 is an all-in-one, NS Geode low power PC/104 CPU board. This user's manual provides information on the physical features, installation, and BIOS setup of the VS-2510.

Built to unleash the total potential of the Pentium Processor, the VS-2510 is all-in-one CPU board computer capable of handling today's demanding requirements. Able to support 200-300 MHz CPUs, this system board supports 10/100M interface network port, and a 4MB PCI-VGA controller that can support both LCD's and CRT's simultaneously or independently.

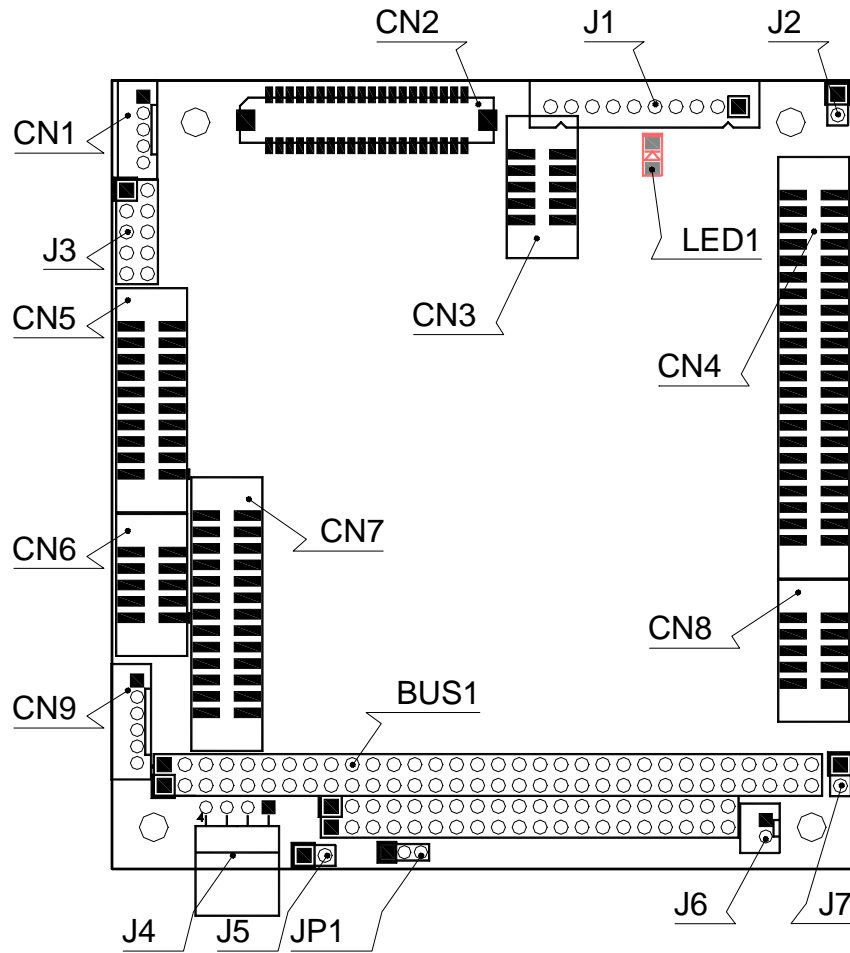
Each VS-2510 has two ports for I/O communications. Two RS-232C ports are available.

The VS-2510 is perfect for POS and POI applications, network systems, panel / MMI's, order entry kiosks, test equipment, OEM projects or as a motherboard for a panel PC. The unit is only 90 X 96 mm, offering unparalleled performance in a very small footprint.

Series Comparison Table

Model	VS-2510
Processor	GX1-300Mhz
Chipset	CS5530A
1 So-DIMM Socket (Max. SDRAM)	128MB
VGA CRT/LCD	CS5530A
Watchdog Timer	Yes
Multi I/O Chip	2S1P
Enhanced IDE	Yes
USB	Yes
Ethernet (10/100Mbps)	One
Board Size	90mm x 96mm

Layout



Specifications

- ❑ Supports 200~300 MHz NS Geode GX1 CPU.
- ❑ NS CS5530 (A) chipset with UMA architecture.
- ❑ 1 So-DIMM socket for up to 128MB PC-100 SDRAM
- ❑ One 100M/10M Ethernet port.
- ❑ Provides CRT, LCD interface with 1.5MB to 4MB shared memory.
- ❑ 1 parallel port, 2 RS-232, 1 floppy port and 1 PCI IDE interface.
- ❑ PS/2 compatible keyboard and mouse interface.
- ❑ Provides header for external speaker.
- ❑ Software programmable watchdog timer.
- ❑ 2 USB ports.
- ❑ Power requires +5V only, 1.2A maximum. (Base on 300MHz CPU and without LCD panel and LCD inverter)
- ❑ EMI Considered on every output signals.
- ❑ PC/104 form factor, 90.2 mm x 95.9 mm (3.55" x 3.775")

Packing List

Upon receiving the package, verify the following things. Should any of the mentioned happens, contact us for immediate service.

- Unpack and inspect the VS-2510 package for possible damage that may occur during the delivery process.
- Verify the accessories in the package according to the packing list and see if there is anything missing or incorrect package is included.
- If the cable(s) you use to install the VS-2510 is not supplied from us, please make sure the specification of the cable(s) is compatible with the VS-2510 system board.

Note: after you install the VS-2510 series, it is recommended that you keep the diskette or CD that contains drivers and document files, and keep the document copies, or unused cables in the carton for future use.

The following lists the accessories that may be included in your VS-2510 package. Some accessories are optional items that are only shipped upon order.

- One VS-2510 all-in-one PC/104 CPU board.
- One VGA (CRT interface) adapter cable.
- One 44-pin hard disk driver interface cable.
- One 20-pin to 34-pin floppy disk interface cable.
- Two serial port adapter cable and 1 parallel port interface cable. (10-pin IDC to DB-9)
- One PS/2 mouse port adapter cable
- One USB adapter cable with bracket. (Optional)
- One LAN adapter with VS-4605A transfer board
- One compact disk includes software utility.

Chapter 2 Hardware Installation

To set up a VS-2510 system board, complete the description in Chapter 2 and Chapter 3.

This chapter introduces the system board connectors & jumper settings, and guides you to apply them for field application.

Before Installation

Before you install the system board, make sure you follow the following descriptions.

1. Before removing the board from its anti-static bag, wear an anti-static strap to prevent the generation of Electricity Static Discharge (ESD). The ESD may be created from human body that touches the board. It may do damage to the board circuit.
2. Install or unplug any connector, module, or add-on card, be sure that the power is disconnected from the system board. If not, this may damage the system board components, module, or the add-on-card.
3. Installing a heat sink is necessary for heat dissipation from your CPU. If heat sink is not mounted, this may cause the CPU fail due to over-heating problem.

Hardware Features

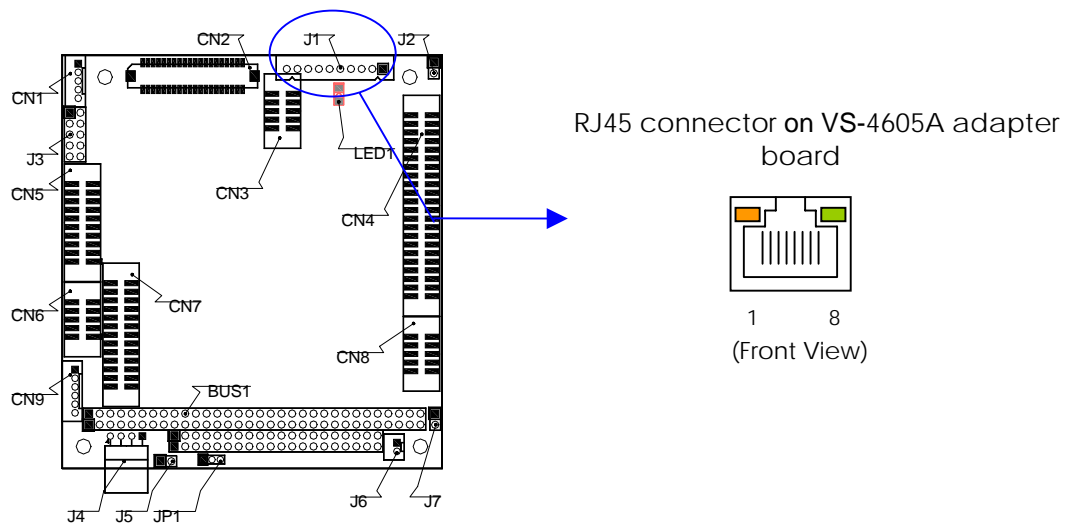
Index to Connectors/Jumpers/Others

The following lists the connectors and jumpers to install the VS-2510.

Item	Description
CN1	Control signals and power source for LCD inverter.
CN2	18-bit LCD interface connector
CN3	CRT connector
CN4	IDE hard disk connectors
CN5	Floppy connector
CN6 & CN8	RS232 connector for serial port 1 and 2
CN7	Parallel port connector
CN9	6-pin 2.0mm keyboard and mouse connector
J1	10-pin LAN port connector
J2	External Speaker Header
J3	USB connector header
J4	Power Connector
J5	Reset header
J6 & JP1	External Battery Header and Battery Select Jumper
J7	External HDD LED Header
BUS1	PC/104 Connector
LED1	Power/Watchdog LED
DIMM1	So-DIMM Socket

J1: RJ45 LAN /Adapter Connector with LED indicators

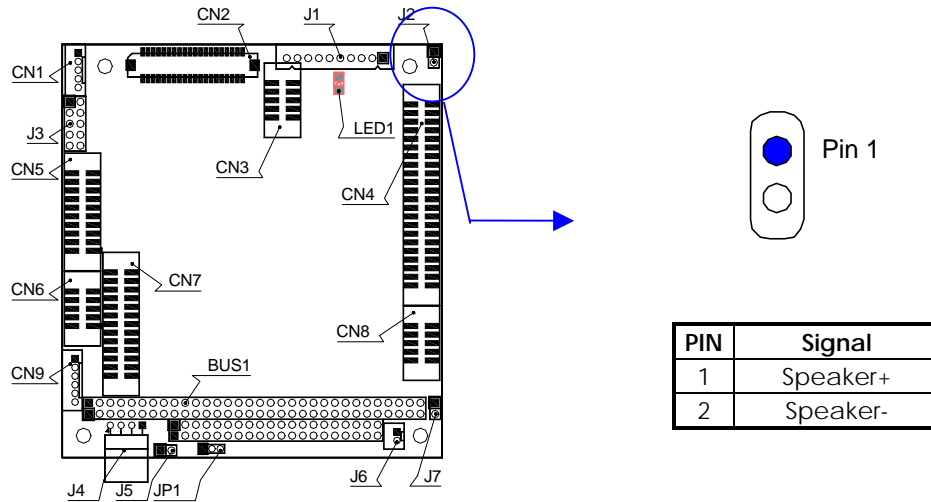
VS-4605A is a RJ45 connector with 2 LEDs for LAN. The left side LED (orange) indicates data is being accessed and the right side LED (green) indicates on-line status. (On indicates on-line and off indicates off-line) J1 provide twist-pair signals of LAN port if you got LAN version and adapter board (VS-4605A) with cable. The following table lists the pin assignments of J1 to RJ45 connector on the VS-4605A LAN adapter board:



The following lists the pin assignment of J1.

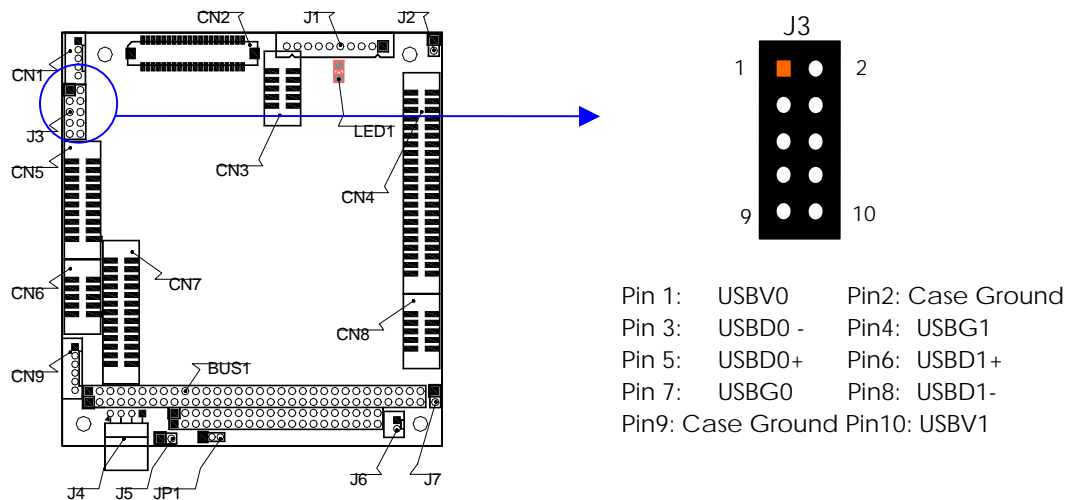
J1	Signal	RJ45	J1	Signal	RJ45
1	TPTX+	1	6	Access LED	-
2	TPTX -	2	7	On-Line LED	-
3	TPRX+	3	8	Case GND	-
4	TPRX -	6	9	FBG1	4
5	LED Common	-		FBG1	5
				FBG2	7
			10	FBG2	8

J2: External Speaker Header

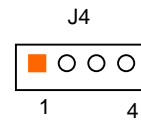
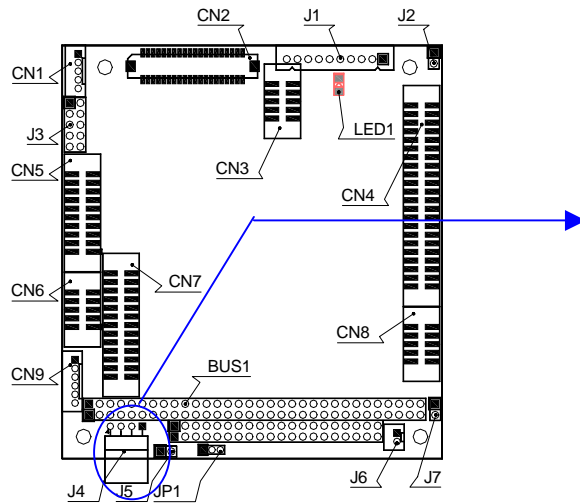


J3: USB Connector

J3 is a dual port USB connector. Any USB device can be attached to J3 with plug-and-play supported.



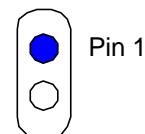
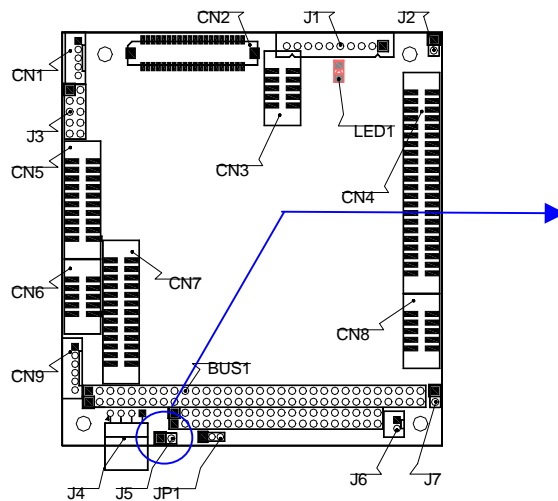
J4: Power Connector (4-pin 2.5mm JST)



Pin 1: VCC (+5V)
Pin 2: Ground
Pin 3: Ground
Pin 4: VDD (+12V)

J5: Reset Header

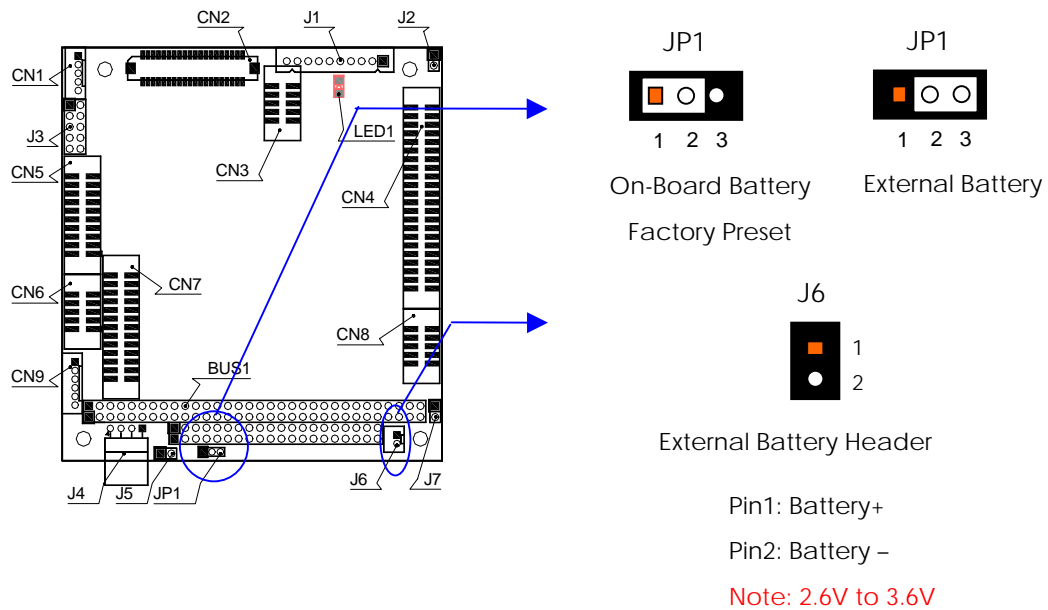
J5 is a 2-pin header for connecting to system reset bottom. Short-circuit these 2 pins to hardware reset VS-2510 as well as restart system. It is similar to power off the system and then power it on again.



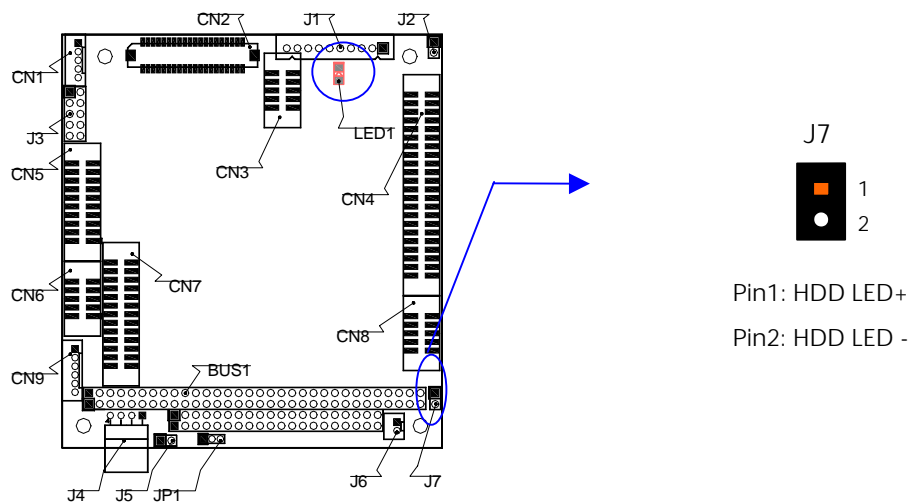
Pin 1: Reset +
Pin 2: Reset -

J6 & JP1: External Battery Header and Battery Select Jumper

J6 is used to connect an external battery pack if on-board Lithium battery is empty or not and please setting JP1 properly of on-board battery or external battery.

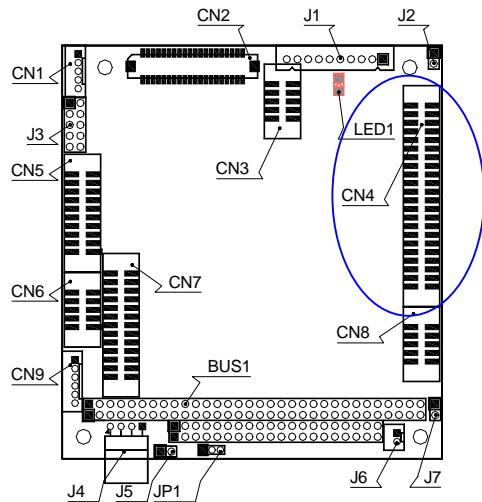


LDE1: Power/Watchdog & J7: External HDD LED Header

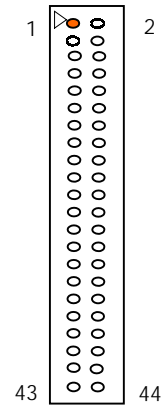


CN4: IDE hard Disk Connectors

CN4 is 44-pin 2.0mm IDC connectors. Use the included hard disk cables to attach up to two 2.5" hard disk drives.



CN4 – Hard disk connector

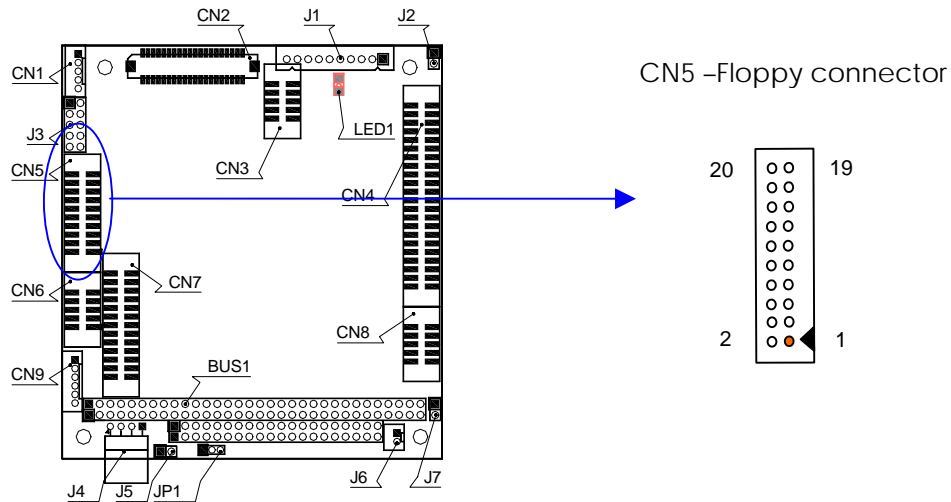


The following table lists the pin description of CN4.

Pin	Description	Pin	Description
1	-RESET	2	GROUND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	GROUND	20	NOT USED
21	IDEDREQ	22	GROUND
23	-IOW A	24	GROUND
25	-IOR A	26	GROUND
27	IDEIORDYA	28	GROUND
29	-DACKA	30	GROUND
31	AIN	32	GROUND
33	SA 1	34	Not Used
35	SA 0	36	SA 2
37	CS 0	38	CS 1
39	HD LED A	40	GROUND
41	VCC	42	VCC
43	GROUND	44	Not Used

CN5: 20-pin Floppy Connector

The included floppy drive interface cable is used to transfer 20-pin connector into standard 34-pin connector. The following table shows signal connections between 20-pin & 34-pin connectors.

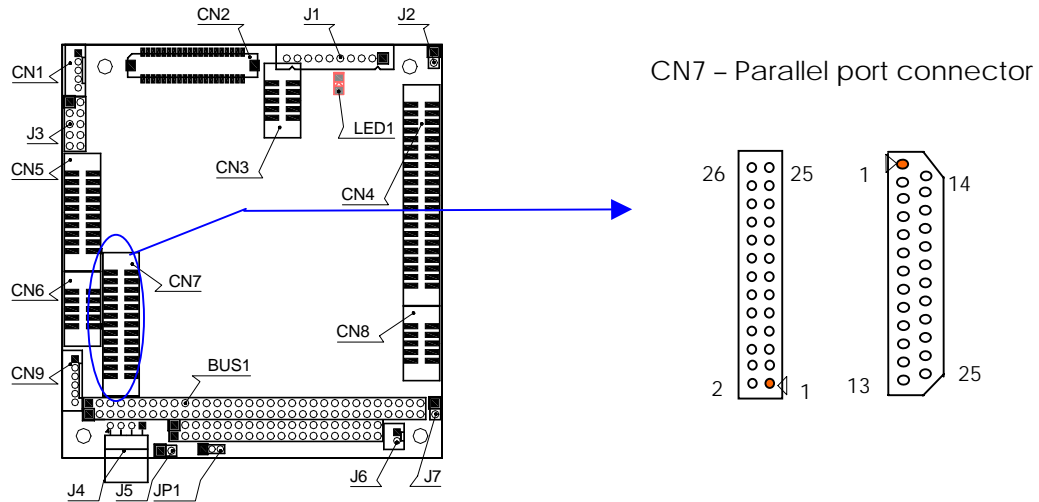


The following table shows signal connections.

20-pin	Signal	34-pin	20-pin	Signal	34-pin
1	Drive Enable A	2	12	Ground	23
2	-Index	8	13	-Write Enable	24
3	-Select A	12	14	-Track 0	26
4	Ground	11	15	-Write Protect	28
5	-Motor A	16	16	Ground	29
6	- Select B	14	17	-Read Data	30
7	-Motor B	10	18	-Head	32
8	Ground	9	19	-Disk Change	34
9	-Direction	18	20	Ground	31
10	-Step	20			
11	-Write Data	22	-	No Connection	Others

CN7: 26-pin Parallel Port Connector (26-pin 2.0mm IDC)

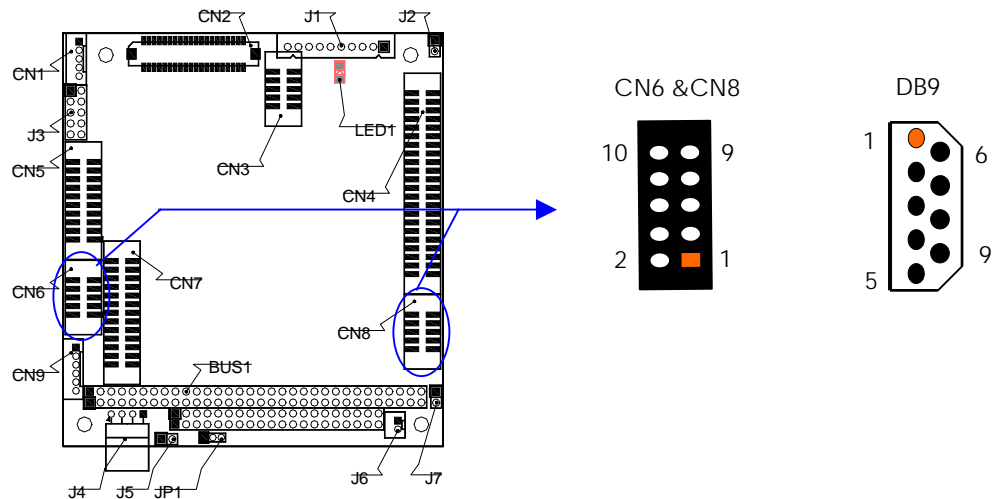
The included printer interface cable is used to transfer 26-pin connector into standard DB25 connector.



CN7	DB-25	Description	CN7	DB-25	Description
1	1	-STROBE	2	14	-AUTO FORM FEED
3	2	DATA 0	4	15	-ERROR
5	3	DATA 1	6	16	-INITIALIZE
7	4	DATA 2	8	17	-PRINTER SELECT IN
9	5	DATA 3	10	18	Ground
11	6	DATA 4	12	19	Ground
13	7	DATA 5	14	20	Ground
15	8	DATA 6	16	21	Ground
17	9	DATA 7	18	22	Ground
19	10	-ACKNOWLEDGE	20	23	Ground
21	11	BUSY	22	24	Ground
23	12	PAPER	24	25	Ground
25	13	PRINTER SELECT	26	--	No Used

CN6 & CN8: Serial Port Connectors RS-232C Pin Definitions

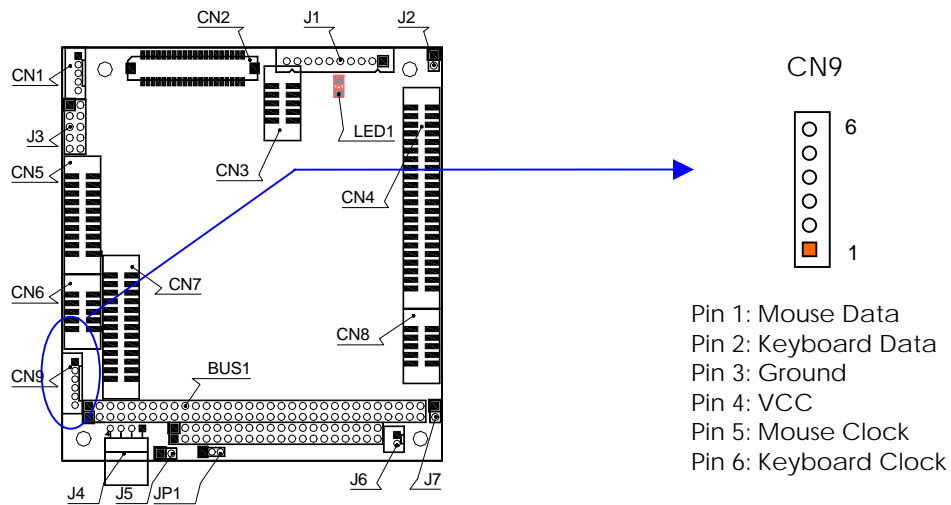
CN6 (COM1) & CN8 (COM2) are 10-pin 2.0mm IDC connectors. The included serial port adapter cables are used to transfer 10-pin 2.0mm IDC into standard DB-9 connector. The following tables show the signal connections of these connectors and the included adapter cable for CN6 & CN8:



CN6 & CN8	RS-232 Signal	DB9
1	-DCD2	1
2	-DSR2	6
3	RXD2	2
4	-RTS2	7
5	-TXD2	3
6	-CTS2	8
7	-DTR2	4
8	-RI2	9
9	GROUND	5
10	GROUND	Shield

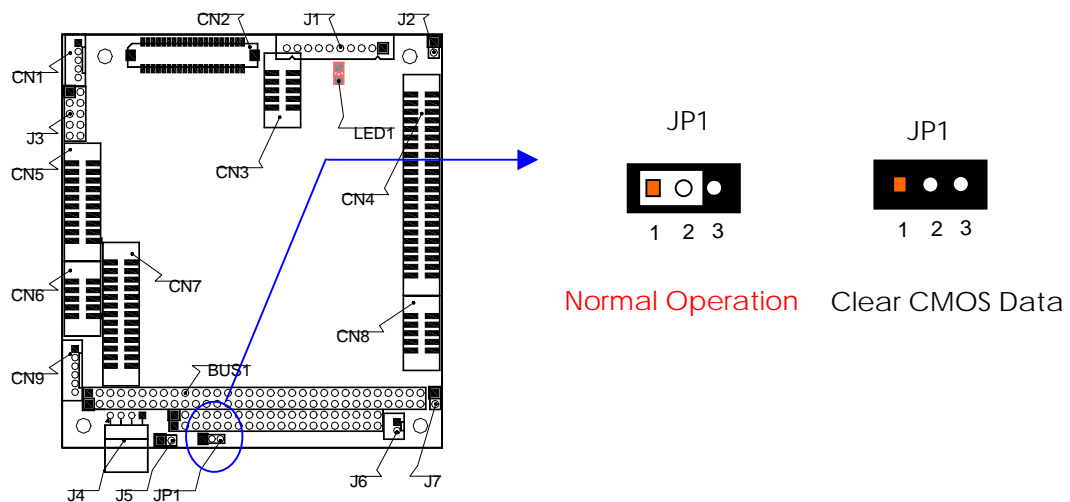
CN9: Keyboard/Mouse Connector

CN9 is a 6-pin 2.0mm JST connector, use the included adapter cable you can attach standard PS/2 type keyboard and mouse.



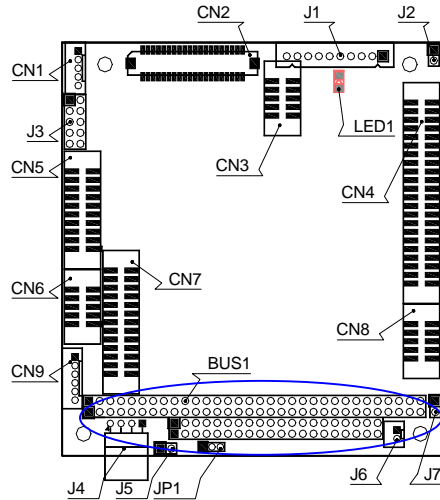
JP1: Clear CMOS Data

You can use JP1 to clear CMOS data. The CMOS store information like system date, time, boot up device, password, IRQ... that are set up with the BIOS. To clear the CMOS, set JP1 to open then return to 1-2 before system is power-off. The default setting is 1-2.

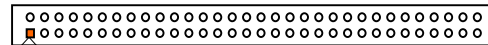


BUS1: PC/104 Bus Connectors

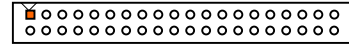
The BUS1 connector supports a little signals of ISA for easy debugging or testing. It is reserved for board manufacture only.



BUS1 – BUS A & B



BUS1 – BUS C & D



PC/104 A&B Pin

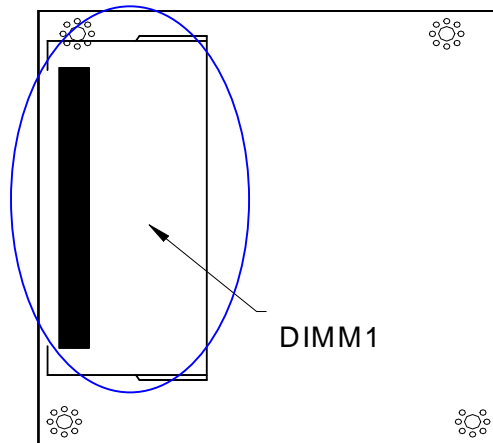
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	-	A17	SA14	B1	Ground	B17	-DACK1
A2	SD7	A18	SA13	B2	RSTDRV	B18	DRQ1
A3	SD6	A19	SA12	B3	+5V	B19	-
A4	SD5	A20	SA11	B4	IRQ9	B20	BUSCLK
A5	SD4	A21	SA10	B5	-5V	B21	IRQ7
A6	SD3	A22	SA9	B6	DRQ2	B22	IRQ6
A7	SD2	A23	SA8	B7	-12V)	B23	IRQ5
A8	SD1	A24	SA7	B8	-ZWS	B24	IRQ4
A9	SD0	A25	SA6	B9	+12V	B25	IRQ3
A10	IORDY	A26	SA5	B10	Key1	B26	-DACK2
A11	AEN	A27	SA4	B11	-MEMW	B27	TC
A12	SA19	A28	SA3	B12	-MEMR	B28	ALE
A13	SA18	A29	SA2	B13	-IOW	B29	+5V
A14	SA17	A30	SA1	B14	-IOR	B30	OSC
A15	SA16	A31	SA0	B15	-DACK3	B31	Ground
A16	SA15	A32	Ground	B16	DRQ3	B32	Ground

PC/104 C& D Pin

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
C1	GND	C11	MEMW#	D1	Ground	D11	-DACK#5
C2	SBHE	C12	SD8	D2	MEMCS16#	D12	DREQ5
C3	LA23	C13	SD9	D3	IOCS16#	D13	DACK#6
C4	LA22	C24	SD10	D4	IRQ10	D14	DREQ6
C5	LA21	C25	SD11	D5	IRQ11	D15	DACK#7
C6	LA20	C26	SD12	D6	IRQ12	D16	DREQ7
C7	LA19	C27	SD13	D7	IRQ15	D17	VCC
C8	LA18	C28	SD14	D8	IRQ14	D18	-
C9	LA17	C29	SD15	D9	DACK#0	D19	GND
C10	MEMR#	C20	KEY	D10	DREQ0	D20	GND

DIMM1: So-DIMM Socket

The DIMM1 socket on the solder side accepts 32MB to 128MB PC-100 SDRAM modules.



Chapter 3 Installing CRT and LCD Monitors

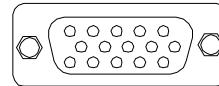
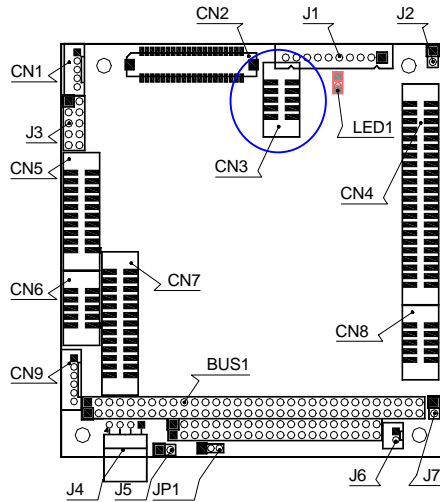
This chapter describes the configuration and installation procedure of LCD and CRT displays. Both CRT and LCD displays may be used at the same time. Only TFT type LCDs may be used. CRT monitors should work with no problem under Windows 95/98. However, each type of LCD requires different BIOS.

The VS-2510 supports a CRT colored monitor and a TFT LCD (DSTN LCDs are not supported with this board). It can be connected to create a compact video solution for the industrial environment. 4MB of RAM on-boarded allows a maximum CRT resolution of 1024X768 with 256 colors and a LCD resolution of 800X600 with 64k colors. Different VGA display modes are possible, but your monitor must possess certain characteristics (different modes require different drivers to display the mode desired).

- LCD Flat Panel Display
- CRT & LCD Display

CRT Display (CN3)

The following table and figure illustrate the pin definition of CN3 and D-sub 15-pin on the CRT adapter cable:



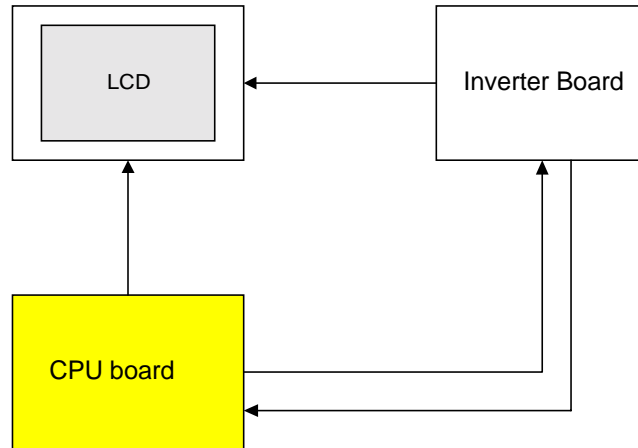
Pin 1: Red
 Pin 2: Green
 Pin 3: Blue
 Pin 13: Hsync
 Pin 14: Vsync
 Pin 12: DDC Data
 Pin 15: DDC Clock
 Pin 5 & 10: Digital Ground
 Pin 6,7,8: Analog Ground
 Others: Not Used

CN3	Signal	DB-15	CN3	Signal	DB15
1	RED	1	6	Case Ground	Case
2	GREEN	2	7	Digital Ground	5,10
3	BLUE	3	8	Analog Ground	6,7,8
4	HSYNC	13	9	DDC Data	12,1
5	VSNC	14	10	DDC Clock	15

LCD FLAT PANEL DISPLAY

Each LCD model requires specific BIOS in order to work properly. If you want to use a panel that your board was not originally designed for then, please send an email to service@visionsystems.de and state the LCD type and full specification you use.

The following shows the block diagram of using VS-2510 for LCD display.



LCD Panel Block Diagram

The block diagram shows that VS-2510 still needs components to be used with a LCD panel. It needs control for the brightness and the contrast of the LCD panel while inverter board is the one that supplies the high voltage to drive the LCD panel.

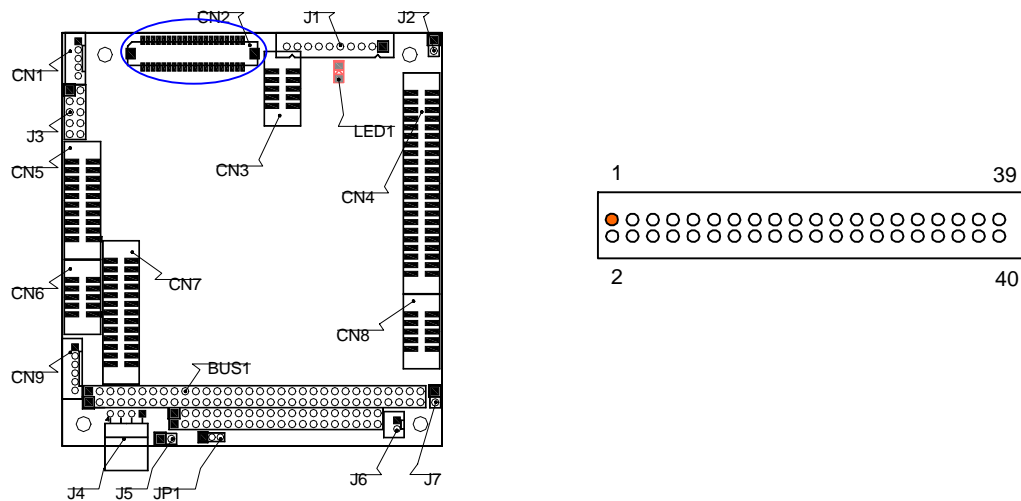
NOTE: Be careful with the pin orientation when installing connectors and the cables. A wrong connection can easily destroy your LCD panel. The pin 1 of the cable connectors is indicated with a sticker and the pin1 of the ribbon cable usually has a different color.

CN2: LCD Connector

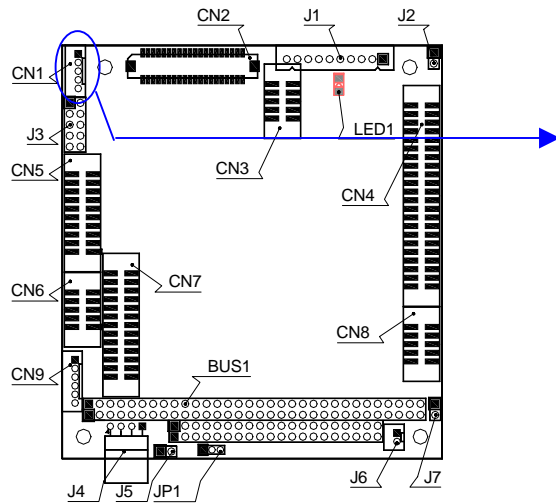
CN2 is an 18-bit LCD interface connector. The pin assignments are listed in the following table.

CN2	Description	CN2	Description	CN2	Description	CN2	Description
1	+5V	21	FPD8	2	+5V	22	FPD9
3	Ground	23	FPD10	4	Ground	24	FPD11
5	+ 3.3V	25	N.C	6	+ 3.3V	26	N.C
7	R/L	27	FPD12	8	Ground	28	FPD13
9	N.C	29	FPD14	10	N.C	30	FPD15
11	FPD0	31	FPD16	12	FPD1	32	FPD17
13	FPD2	33	Ground	14	FPD3	34	Ground
15	FPD4	35	FPCLK	16	FPD5	36	FPVSYNC
17	N.C	37	FPDISP	18	N.C	38	FPHSYNC
19	FPD6	39	U/D	20	FPD7	40	FPVDDEN

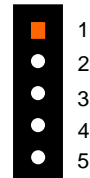
Note: N.C. means not connected, it is reserved for upgraded signals.



CN1 provides control signals and power source for LCD inverter.



CN1



Pin1: +12V
Pin2: Ground
Pin3: FPBLKEN
Pin4 VR.
Pin5: +5V

Note: +12V is come from J4 only

Chapter 4 BIOS Setup

This chapter describes the BIOS setup.

Overview

BIOS are a program located on a Flash memory chip on a circuit board. It is used to initialize and set up the I/O peripherals and interface cards of the system, which includes time, date, hard disk drive, the ISA bus and connected devices such as the video display, diskette drive, and the keyboard. This program will not be lost when you turn off the system.

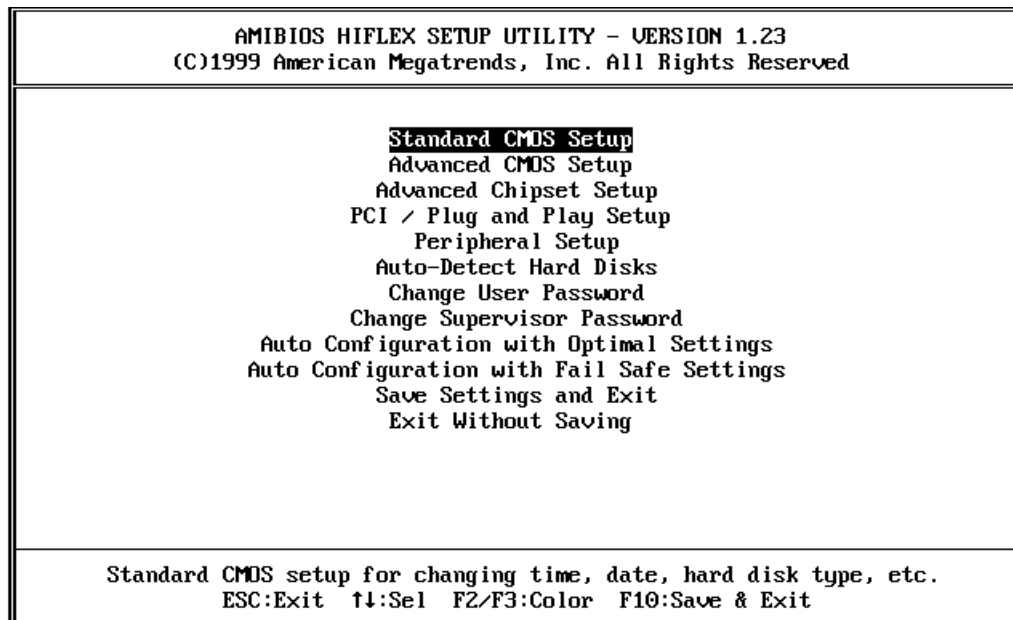
The BIOS provides a menu-driven interface to the console subsystem. The console subsystem contains special software, called firmware that interacts directly with the hardware components and facilitates interaction between the system hardware and the operating system.

The BIOS default values ensure that the system will function at its normal capability. In the worst situation the user may have corrupted the original settings set by the manufacturer.

All the changes you make will be saved in the system RAM and will not be lost after power-off.

When you start the system, the BIOS will perform a self-diagnostics test called Power On Self Test (POST) for all the attached devices, accessories, and the system. Press the [Del] key to enter the BIOS Setup program, and then the main menu will show on the screen.

Note: Change the parameters when you fully understand their functions and subsequence.



BIOS Functions

On the menu, you can perform the following functions

1. Standard CMOS Setup- Advanced CMOS Setup
2. Advanced Chipset Setup
3. PCI/ Plug and Play Setup
4. Peripheral Setup
5. Hardware Monitor Setup
6. Auto-Detect Hard Disks
7. Change User Password
8. Change Supervisor Password
9. Auto Configuration with Optimal Settings: to auto configure the system according to optimal setting with pre-defined values. This is also the factory default setting of the system when you receive the board.
10. Auto Configuration with Fail Safe Settings: to configure the system in fail-safe mode with predefined values.
11. Save Settings and Exit: perform this function when you change the setting and exit the BIOS Setup program.
12. Exit without saving: perform this function when you want to exit the program and do not save the change.

Keyboard Convention

On the BIOS, the following keys can be used to operate and manage the menu:

Item	Function
ESC	To exit the current menu or message
Page Up/Page Down	To select a parameter
F1	To display the help menu if you do not know the purpose or function of the item you are going to configure
F2/F3	To change the color of the menu display. F2 is to go forward and F3 to go backward
UP/Down Arrow Keys	To go upward or downward to the desired item

STANDARD CMOS SETUP

This section describes basic system hardware configuration, system clock setup and error handling. If the CPU board is already installed in a working system, you will not need to select this option anymore.

AMIBIOS SETUP - STANDARD CMOS SETUP											
(C)2000 American Megatrends, Inc. All Rights Reserved											
Date (mm/dd/yyyy): Fri Apr 27, 2001						Base Memory: 0 KB					
Time (hh/mm/ss) : 17:09:39						Extd Memory: 0 MB					
Floppy Drive A:		1.44 MB 3½									
Floppy Drive B:		Not Installed									
Type		Size	Cyls	Head	WPcom	Sec	LBA Mode	Blk Mode	PIO Mode	32Bit Mode	
Pri Master: Auto											Off
Pri Slave : Auto											Off
Boot Sector Virus Protection						Disabled					
Month: Jan - Dec						ESC:Exit ↑↓:Sel					
Day: 01 - 31						PgUp/PgDn:Modify					
Year: 1901 - 2099						F1:Help F2/F3:Color					

☐ Date & Time Setup

Highlight the <Date> field and then press the [Page Up] / [Page Down] or [+] / [-] keys to set the current date. Follow the month, day and year format.

Highlight the <Time> field and then press the [Page Up] / [Page Down] or [+] / [-] keys to set the current date. Follow the hour, minute and second format.

The user can bypass the date and time prompts by creating an AUTOEXEC.BAT file. For information on how to create this file, please refer to the MS-DOS manual.

☐ Floppy Setup

The <Standard CMOS Setup> option records the types of floppy disk drives installed in the system.

To enter the configuration value for a particular drive, highlight its corresponding field and then select the drive type using the left-or right-arrow key.

☐ Hard Disk Setup

The BIOS supports various types for user settings, The BIOS supports <Pri Master>, <Pri Slave>, <Sec Master> and <Sec Slave> so the user can install up to four hard disks.

For the master and slave jumpers, please refer to the hard disk's installation descriptions and the hard disk jumper settings.

You can select <AUTO> under the <TYPE> and <MODE> fields. This will enable auto detection of your IDE drives during boot up. This will allow you to change your hard drives (with the power off) and then power on without having to reconfigure your hard drive type. If you use older hard disk drives, which do not support this feature, then you must configure the hard disk drive in the standard method as described above by the <USER> option.

☐ **Boot Sector Virus Protection**

This option protects the boot sector and partition table of your hard disk against accidental modifications. Any attempt to write to them will cause the system to halt and display a warning message. If this occurs, you can either allow the operation to continue or use a bootable virus-free floppy disk to reboot and investigate your system. The default setting is <*Disabled*>. This setting is recommended because it conflicts with new operating systems. Installation of new operating system requires that you disable this to prevent write errors.

ADVANCED CHIPSET SETUP

This section describes the configuration entries that allow you to improve your system performance, or let you set up some system features according to your preference. Some entries here are required by the CPU board's design to remain in their default settings.

AMIBIOS SETUP - ADVANCED CMOS SETUP (C)1999 American Megatrends, Inc. All Rights Reserved		
Quick Boot	Enabled	Available Options: ► Read-Write Read-Only
1st Boot Device	1st IDE-HDD	
2nd Boot Device	Floppy	
3rd Boot Device	ATAPI CDROM	
Floppy Access Control	Read-Write	
Hard Disk Access Control	Read-Write	
BootUp Num-Lock	On	
Floppy Drive Swap	Disabled	
Floppy Drive Seek	Disabled	
PS/2 Mouse Support	Enabled	
System Keyboard	Absent	
Primary Display	Absent	
Password Check	Setup	
Wait For 'F1' If Error	Disabled	
Hit 'DEL' Message Display	Enabled	
C000,16k Shadow	Cached	
C400,16k Shadow	Cached	
C800,16k Shadow	Disabled	
CC00,16k Shadow	Disabled	
D000,16k Shadow	Disabled	
D400,16k Shadow	Disabled	
D800,16k Shadow	Disabled	
DC00,16k Shadow	Disabled	

ESC:Exit F1:Sel
PgUp/PgDn:Modify
F1:Help F2/F3:Color

☐ Quick Boot

This field is used to activate the quick boot function of the system. When set to Enabled,

1. BIOS will not wait for up to 40 seconds if a Ready signal is not received from the IDE drive, and will not configure its drive.
2. BIOS will not wait for 0.5 seconds after sending a RESET signal to the IDE drive.
3. You cannot run BIOS Setup at system boot since there is no delay for the Hit, Del. To run Setup message.

Available Options: Disabled, Enabled

Default setting: Enabled

☐ 1st -3rd Boot Device

These fields determine where the system attempts to look for the boot drive priority for an operating system. The default procedure is to check the hard disk, and then the floppy drive, and last the CDROM.

Available options: Disabled, IDE0-1, IDE-2, IDE-3, Floppy, ARMD-FDD, ARMD-HDD, CDROM, and SCSI, Network

Default setting: IDE-0 for 1st Boot device; Floppy for 2nd Boot Device; CDROM for 3rd Boot Device

□ **Floppy Access Control**

This field specifies the read/write access when booting from a floppy drive.

Available options: Normal, Read-only

Default setting: Normal

□ **Hard Disk Access Control**

This field specifies the read/write access when booting from a HDD drive.

Available options: Normal, Read-only

Default setting: Normal

□ **S.M.A.R.T for Hard Disk**

This field is used to activate the S.M.A.R.T (System Management and Reporting Technologies) function for S.M.A.R.T HDD drives. This function requires an application that can give S.M.A.R.T message.

Available options: Disabled, Enabled

Default: Disabled

□ **Boot Up Numlock**

This field is used to activate the Num Lock function upon system boot. If the setting is on, after a boot, the Num Lock light is lit, and user can use the number key.

Available options: On, Off

Default setting: On

□ **Floppy Drive Swap**

The field reverses the drive letter assignments of your floppy disk drives in the Swap A, B setting, otherwise leave on the default setting of ***Disabled*** (No Swap). This works separately from the BIOS Features floppy disk swap feature. It is functionally the same as physically interchanging the connectors of the floppy disk drives. When the function's setting is ***<Enabled>***, the BIOS swapped floppy drive assignments so that Drive A becomes Drive B, and Drive B becomes Drive A under DOS.

Available options: Disabled, Enabled

Default setting: Disabled

☐ **Floppy Drive Seek**

This field is used to set if the BIOS will seek the floppy <A> drive upon boot.

Available Options: Disabled, Enabled

Default setting: Disabled

☐ **PS/2 Mouse Support**

The PS/2 mouse function is optional. Before you configure this field, make sure your VS-2510 supports this feature. The setting of **Enabled** allows the system to detect a PS/2 mouse on boot up. If detected, IRQ12 will be used for the PS/2 mouse. IRQ 12 will be reserved for expansion cards if a PS/2 mouse is not detected. **Disabled** will reserve IRQ12 for expansion cards and therefore the PS/2 mouse will not function.

Available options: Disabled, Enabled

Default setting: Enable

☐ **Typematic rate**

This function specifies the keystroke repeat rate when a key is pressed and held down.

Available options: Fast, Slow

Default setting: Fast

☐ **System Keyboard**

This field specifies if an error message should be prompted when a keyboard is not attached.

Available options: Absent, Present

Default setting: Absent

☐ **Primary Display**

The field specifies the type of monitor installed in the system.

Available options: Absent, VGA/EGA, CGA40x25, CGA80x25, and Mono

Default setting: Absent

☐ **Password Check**

This field enables password checking every time the computer is powered on or every time the BIOS Setup is executed. If **Always** is chosen, a user password prompt appears every time and the BIOS Setup Program executes and the computer is turned on. If **Setup** is chosen, the password prompt appears if the BIOS executed.

Available options: Setup, Always

Default setting: Setup

☐ **Boot To OS2> 64MB**

If OS2 operating system is used, and the system RAM is over 64MB, please select yes. Otherwise, select No.

Available options: Yes, No

Default setting: No

☐ **Wait for 'F1' If Error**

AMIBIOS POST error messages are followed by:

Press <F1> to continue

If this field is set to **Disabled**, the AMIBIOS does not wait for you to press the <F1> key after an error message.

Available options: Disabled, Enabled

Default setting: Disabled

☐ **Hit 'DEL' Message Display**

Set this field to **Disabled** to prevent the message as follows:

Hit 'DEL' if you want to run setup

It will prevent the message from appearing on the first BIOS screen when the computer boots.

Available options: Disabled, Enabled

Default setting: Enabled

□ **C000, 32k Shadow - E800, 32k shadow**

These fields control the location of the contents of the 32KB of ROM beginning at the specified memory location. If no adapter ROM is using the named ROM area, this area is made available to the local bus. The settings are:

1. **Disabled:** The video ROM is not copied to RAM. The contents of the video ROM cannot be read from or written to cache memory.
2. **Enabled:** The contents of C000h - C7FFFh are written to the same address in system memory (RAM) for faster execution.
3. **Cached:** The contents of the named ROM area are written to the same address in system memory (RAM) for faster execution, if an adapter ROM will be using the named ROM area. Also, the contents of the RAM area can be read from and written to cache memory.

Available options: Disabled, Enabled, Cached

Default setting: Disabled

ADVANCED CHIPSET SETUP

This section describes the configuration of the board's chipset features.

AMIBIOS SETUP - ADVANCED CHIPSET SETUP (C)1999 American Megatrends, Inc. All Rights Reserved		
Video Memory Size	1.5 MB	Available Options: Disabled ▶ 1.5 MB 2.5 MB 4.0 MB
LCD CRT Selection	CRT	
LCD Type	640×480	
IO Recovery Time	32 Clock	
L1 Scratch Pad	3 Kb	
Enable GXM SDRAM Options	Disabled	
CAS Latency	3	
tRC Bits 24-27 TIM1	3	
tRAS Bits 20-23 TIM1	7	
SDRAM Clock Ratio	3.0	
SDRAM Clock Shift	1.5	
USB Function	Enabled	
		ESC:Exit ↑↓:Sel PgUp/PgDn:Modify F1:Help F2/F3:Color

☐ Video Memory Size

This field specifies which VGA display memory. You can select either Video memory on the VGA. The setting are share onboard memory.

Available Options: 1.5MB, 2.5MB, and 4MB

Default setting: 1.5MB

☐ LCD CRT Selection

This field specifies which VGA display will be used when the system is boot. You can select either the LCD or the CRT booting on the VGA.

Available Options: Both, LCD, and CRT

Default setting: CRT

❑ **LCD Type**

When use the LCD the field specifies which select display resolution for different TFT LCD display type.

Available Options: 640x480, 800x600 and 1024x768

Default setting: 640X480

❑ **I/O Recovery Time**

The recovery time is the length of time, measured in CPU clocks, which the system will delay after achieving an input/output request. This delay takes place to wait for the I/O to complete the request. This field specifies the recovery time for I/O.

Available Options: No Delay, 2, 4, 8,16, 32, 64 and 128 Clock

Default setting: 32 Clock

❑ **L1 Scratch Pad**

This Scratch RAM operates at L1 speed that can speed up time-critical softer operations.

Available Options: 2 Kb and 3Kb

Default setting: 2/2 SCLKS

❑ **Enable GXM SDRAM Option**

This field is control signals item of the Synchronous SDRAM system access cycle when SDRAM is installed.

Available Options: Disable, Enable

Default setting: Disable

❑ **CAS Latency**

This field specifies the length of the delay inserted between RAS and CAS signals of the Synchronous DRAM system access cycle.

Available Options: 1, 2, 3, 4, 5, 6 and 7

Default setting: 3

☐ **tRC Bits 24-27 TIM1**

This field specifies the SDRAM between refresh and ACT /PRE commands.

Available Options: 2, 3, 4, 5, 6, 7 and 8

Default setting: 3

☐ **tRAS Bits 20-23 TIM1**

This field specifies the SDRAM between refresh and ACT commands.

Available Options: 1, 2, 3, 4, 5, 6 and 7

Default setting: 7

☐ **SDRAM Clock Ratio**

This specifies the SDRAM clock ratio.

Available Options: 2.0, 2.5, 3.0, 3.5, and 4

Default setting: 3.0

☐ **SDRAM Clock Shift**

This specifies the SDRAM clock meet SDRAM setup and hold time requirements.

Available Options: No Shift, 0.5, 1.0, 1.5, 2.0, 2.5, 3.0 and 3.5

Default setting: 1.5

☐ **USB Function**

Select Enabled if a USB device is installed to the system. If Disabled are selected, the system will not be able to use a USB device.

Available Options: Disabled, Enabled

Default setting: Enabled

PCI/PLUG AND PLAY

AMIBIOS SETUP - PCI / PLUG AND PLAY SETUP (C)1999 American Megatrends, Inc. All Rights Reserved		
Plug and Play Aware O/S	No	Available Options: ► No Yes
PCI Latency Timer (PCI Clocks)	64	
PCI VGA Palette Snoop	Disabled	ESC:Exit ↑↓:Sel PgUp/PgDn:Modify F1:Help F2/F3:Color
DMA Channel 0	PnP	
DMA Channel 1	PnP	
DMA Channel 3	PnP	
DMA Channel 5	PnP	
DMA Channel 6	PnP	
DMA Channel 7	PnP	
IRQ3	PCI/PnP	
IRQ4	PCI/PnP	
IRQ5	PCI/PnP	
IRQ7	PCI/PnP	
IRQ9	PCI/PnP	
IRQ10	PCI/PnP	
IRQ11	PCI/PnP	
IRQ14	PCI/PnP	
IRQ15	PCI/PnP	
Reserved Memory Size	Disabled	
Reserved Memory Address	C8000	

☐ **Plug and Plug Aware O/S**

Set to yes to inform BIOS that the operating system can handle Plug and Play (PnP) devices.

Available Options: Yes, No

Default setting: No

☐ **PCI Latency Timer**

This field specifies the latency timings (in PCI clock) PCI devices installed in the PCI expansion bus.

Available Options: 32, 64, 96, 128, 160,192, 224, and 248

Default setting: 64

☐ **PCI VGA Palette Snoop**

When Enabled is selected, multiple VGA devices operating on different buses can handle data from the CPU on each set of palette registers on every video device. Bit 5 of the command register in the PCI device configuration space is the VGA Palette Snoop bit. (0 is disabled).

Available Options:

Disabled: Data read and written by the CPU is only directed to the PCI VGA devices palette registers.

Enabled: Data read and written by the CPU is directed to both the PCI VGA device's palette registers and the ISA VGA device palette registers, permitting the palette registers of both devices to be identical.

Default setting: Disable

□ **DMA Channel 0 – 7**

When I/O resources are controlled manually, you can assign each system DMA as one of the following types, based on the type of device using the interrupt:

ISA/EISA devices comply with the original PC AT bus specification, requiring a specific interrupt (Such as IRQ5 for COM1).

PnP (PCI/ISA) devices: comply with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

Available Options: PnP, ISA/EISA

Default setting: PnP

□ **IRQ 3 –15**

When I/O resources are controlled manually, you can assign each system interrupt as one of the following types, based on the type of device using the interrupt:

ISA/EISA devices comply with the original PC AT bus specification, requiring a specific interrupt (Such as IRQ5 for COM1).

PnP (PCI/ISA) devices: comply with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

□ **Reserved Memory Size**

You can manually reserve a memory size for a certain interface card if required.

Available Options: Disabled, 16K, 32K, 64K

Default setting: Disabled

□ **Reserved Memory Address**

When a memory Reserved Memory Size is enabled, specify an address range within the C8000 and DC000.

Available Options: C0000, C4000, C8000, CC000, D0000, D4000, D8000, DC000.

Default setting: C8000

PERIPHERAL SETUP

This section describes the function of peripheral features.

AMIBIOS SETUP - PERIPHERAL SETUP (C)1999 American Megatrends, Inc. All Rights Reserved		
OnBoard FDC	Auto	Available Options: ▶ Auto Disabled Enabled
OnBoard Serial Port1	3F8h/COM1	
OnBoard Serial Port2	2F8h/COM2	
OnBoard Parallel Port	378h	
Parallel Port Mode	Normal	
EPP Version	N/A	
Parallel Port IRQ	7	
Parallel Port DMA Channel	N/A	
OnBoard IDE	Enabled	
Primary IDE Read Prefetch	Disabled	
Primary IDE Write Buffering	Disabled	
		ESC:Exit F4:Sel PgUp/PgDn:Modify F1:Help F2/F3:Color

☐ **OnBoard FDC**

This field enables the floppy drive controller on the VS-2510.

Available Options: Disabled, Enabled

Default setting: Enabled

☐ **OnBoard Serial Port 1**

These fields select the I/O port address for each Serial port. Refer to Table 2-2.

Available Options: Auto, Disabled, 3F8H/COM1, 2F8H/COM2, and 3E8H/COM3, 2E8H/COM4.

Default setting: 3F8H/COM1

☐ **OnBoard Serial Port 2**

These fields select the I/O port address for each Serial port. Refer to Table 2-2.

Available Options: Auto, Disabled, 3F8H/COM1, 2F8H/COM2, and 3E8H/COM3, 2E8H/COM4.

Default setting: 2F8H/COM2

☐ **OnBoard Parallel Port**

This field selects the I/O port address for parallel port.

Available Options: Auto, Disabled, 378, 278, and 3BCH

Default setting: 378H

☐ **Parallel Port Mode**

This field specifies the parallel port mode. ECP and EPP are both bi-directional data transfer schemes that adhere to the IEEE P1284 specifications.

Available Options: N/A, Normal, Bi-Dir, EPP, and ECP

Default setting: Normal

☐ **EPP Version**

This field specifies the EPP version for the Parallel Port Mode specification used in the system and is not configurable. If Normal or ECP is selected, this field displays N/A, meaning not available.

Available Options: N/A, 1.7, 1.9

Default setting: N/A

☐ **Parallel Port IRQ**

This field specifies the IRQ for the parallel port.

Available Options: Auto, N/A, 5, 7

Default setting: IRQ7 for Parallel Port; IRQ5 for Parallel Port 2

☐ **Parallel Port DMA Channel**

This option is only available if the setting for the parallel Port Mode option is ECP.

Available Options: N/A, 0,1,3

Default setting: N/A

☐ **OnBoard IDE**

This field specifies the IDE channel that can be applied when using CN3 IDE hard disk connector.

Available Options: Disabled, Enable

Default setting: Enable

Password Setup

There are two security passwords: Supervisor and User. Supervisor is a privileged person that can change the User password from the BIOS.

According to the default setting, both access passwords are not set up and are only valid after you set the password from the BIOS.

To set the password, please complete the following steps.

1. Select **Change Supervisor Password**.
2. Type the desired password (up to 8 character length) when you see the message, "Enter New Supervisor Password."
3. Then you can go on to set a user password (up to 8 character length) if required. Note that you cannot configure the User password until the Supervisor password is set up.
4. Enter Advanced CMOS Setup screen and point to the Password Checkup field.
5. Select Always or Setup.
 - ✧ **Always:** a visitor who attempts to enter BIOS or operating system will be prompted for password.
 - ✧ **Setup:** a visitor who attempts to the operating system will be prompted for user password. You can enter either User password or Supervisor password.
6. Point to **Save Settings and Exit** and press Enter.
7. Press Y when you see the message, "Save Current Settings and Exit (Y/N)?"

Note: it is suggested that you write down the password in a safe place to avoid that password may be forgotten or missing.

To set the password, please complete the following steps.

1. Select **Change Supervisor Password**.
2. Press Enter instead of entering any character when you see the message, "Enter New Supervisor Password."
3. Thus you can disable the password.

Chapter 5 Driver and Utility

The enclosed diskette includes VS-2510 VGA and LAN driver.

VGA Drivers

WIN98/WIN95 Driver

- 1 To install the VGA driver, insert the CD ROM into the CD ROM device, and enter DRIVER>VGA>NS5530>WIN98. If your system is not equipped with a CD ROM device, copy the VGA driver from the CD ROM to a 1.44" diskette.
- 2 Execute CYRIXM-1.exe file.
- 3 The screen shows the SETUP type. Press any key to enter the main menu.
- 4 As the setup is completed, the system will generate the message as follows.

Yes, I want to restart my computer now. Installation is done!

No, I will restart my computer later.

System must be restart then complete the installation.

- 5 In the WINDOWS98/ME, you can find the <DISPLAYL> icon located in the {CONTROL PANEL} group.
- 6 Adjust the <Resolution> and <Color>.

LAN Utility & Driver

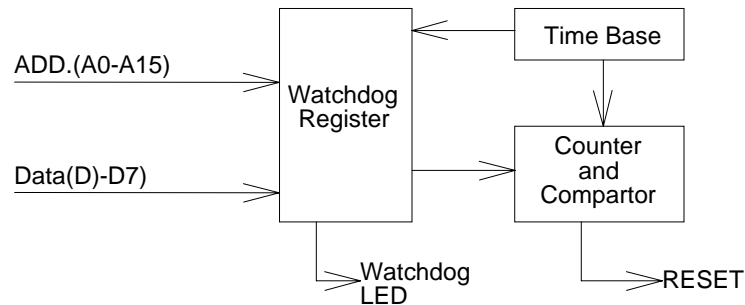
- 1 To install the LAN utility OR driver, insert the CD ROM into the CD ROM device, and enter DRIVER>LAN>RTL8139C. If your system is not equipped with a CD ROM device, copy the LAN VGA driver from the CD ROM to a 1.44" diskette.
- 2 Execute install.exe file.

Note: In the LAN directory, a HELPM.EXE file is included to provide installation information

Watchdog Timer

This section describes how to use the Watchdog Timer, including disabled, enabled, and trigger functions.

The VS-2510 is equipped with a programmable time-out period watchdog timer. You can use your own program to enable the watchdog timer. Once you have enabled the watchdog timer, the program should trigger the I/O every time before the timer times out. If your program fails to trigger or disable this timer before it times out, e.g. because of a system hang-up, it will generate a reset signal to reset the system. The time-out period can be programmed to be set from 1 to 255 seconds or minutes.



The CD -ROM includes a Watch Dog demo file. In the file, there are 3 execution programs written in different forms. The sub-directories of the file are:

1. WATCHDOG/ASSEMBLE: Library and Test Program written in Assembly Language
2. WATCHDOG/TURBOC: Library and Test Program written in Turbo C++

The WATCHDOG includes a demonstration program established for users who would like to configure the Watchdog timer by themselves.

Note: In the WATCHDOG directory, README.TXT file is included to provide demo program information.

Watchdog Timer Setting

The watchdog timer is a circuit that may be used from your program software to detect system crashes or hang-ups. LED1 on this CPU board is the watchdog timer indicator, which is located at the upper-right corner above the USB connector. Whenever the watchdog timer is enabled, the LED will blink to indicate that the timer is counting. The watchdog timer is automatically disabled after reset.

Once you have enabled the watchdog timer, your program must trigger the watchdog timer every time before it times out. After you trigger the watchdog timer, it will be set to non-zero value to watchdog counter and start to count down again. If your program fails to trigger the watchdog timer before time-out, it will generate a reset pulse to reset the system.

The factor of the watchdog timer time-out constant is approximately 1 seconds. The period for the watchdog timer time-out is between 1 to FF timer factors.

If you want to reset your system when watchdog times out, the following table listed the relation of timer factors between time-out periods.

Time Factor	Time-Out Period (Seconds)	Time-Out Period (Minutes)
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
"	"	"
"	"	"
"	"	"
FF	FF	FF

Watchdog Timer Enabled

To enable the watchdog timer, you have to output a byte of timer factor to the watchdog. The following is a Turbo C++ program, which demonstrates how to enable the watchdog timer and set the time-out period at 6 seconds.

```
#include "stdio.H"
#include "WDLIB.H"

main()
{
    char WD_TIME=0x6;

    InitWD(equWdUnitS);
    printf ("Enable watchdog");
    //Triggers watchdog Timer Output is 6 seconds
    EnWD(WD_TIME);
}
```

Watchdog Timer Trigger

After you enable the watchdog timer, your program must write the same factor as enabling to the watchdog register at least once every time-out period to its previous setting. You can change the time-out period by writing another timer factor to the watchdog register at any time, and you must trigger the watchdog before the new time-out period in the next trigger. Below is a Turbo C++ program, which demonstrates how to trigger the watchdog timer:

```
#include "stdio.H"
#include "WDLIB.H"

main()
{
    char WD_TIME=0x6;

    InitWD(equWdUnitS);
    printf ("Enable watchdog");
    //Triggers watchdog Timer Output is 6 seconds
    EnWD(WD_TIME);
}
```

Watchdog Timer Disabled

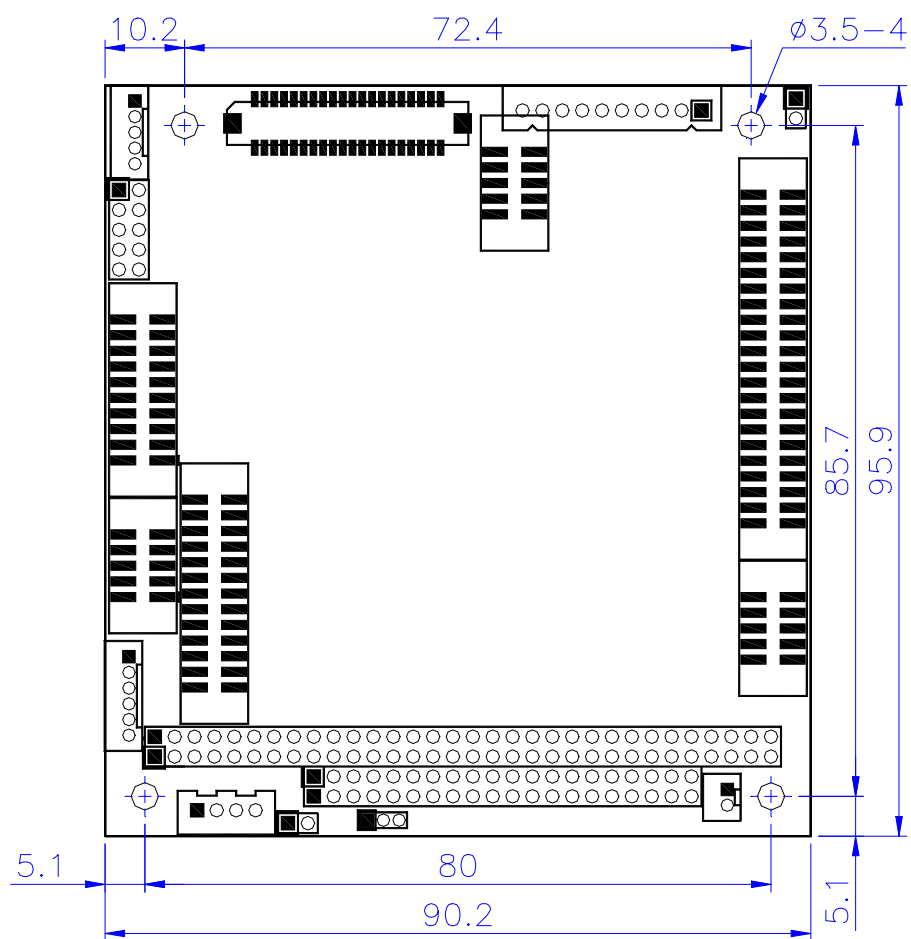
To disable the watchdog timer, simply write a 00H to the watchdog register.

```
#include "stdio.H"
#include "WDLIB.H"

main()
{
    InitWD(equWdUnitS);
    printf ("Disable Watch Dog");
    //Disable watch dog
    DisWD(WD_TIME);
}
```

Appendix

Dimension



Technical Reference

Real-Time Clock and Non-Volatile RAM

The VS-2510 contains a real-time clock compartment that maintains the date and time in addition to storing configuration information about the computer system. It contains 14 bytes of clock and control registers and 114 bytes of general purpose RAM. Because of the use of CMOS technology, it consumes very little power and can be maintained for long periods of time using an internal Lithium battery. The contents of each byte in the CMOS RAM are listed below:

Address	Description
00	Seconds
01	Second alarm
02	Minutes
03	Minute alarm
04	Hours
05	Hour alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	Diagnostic status byte
0F	Shutdown status byte
10	Diskette drive type byte, drive A and B
11	Fixed disk type byte, drive C
12	Fixed disk type byte, drive D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte

Address	Description
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	Low actual expansion memory byte
31	High actual expansion memory byte
32	Date century byte
33	Information flags (set during power on)
34-7F	Reserved for system BIOS

CMOS RAM Map

Register	Description
00h -10h	Standard AT-compatible RTC and Status and Status Register data definitions
11h – 13h	Varies
14h	Equipment Bits 7-6 Number of Floppy Drives 00 1 Drive 01 2 Drives Bits 5-4 Monitor Type 00 Not CGA or MDA 01 40x25 CGA 01 2 Drives 80x25 CGA Bits 3 Display Enabled 0 Disabled 1 Enabled Bit 2 Keyboard Enabled 00 Not CGA or MDA 01 40x25 CGA 01 2 Drives 80x25 CGA Bit 1 Math Coprocessor Installed 0 Absent 1 Present Bit 0 Floppy Drive Installed 0 Disabled 1 Enabled
15h	Base Memory (in 1KB increments), Low Byte
16h	Base Memory (in 1KB increments), High Byte
17h	IBM-compatible memory (in 1KB increments), Low Byte
18h	IBM-compatible memory (in 1KB increments), High Byte (max 15 MB)
19h-2Dh	Varies
2Eh	Standard CMOS RAM checksum, high byte
2Fh	Standard CMOS RAM checksum, low byte
30h	IBM-compatible Extended Memory, Low Byte (POST) in KB
31h	IBM-compatible Extended Memory, High Byte (POST) in KB
32h	Century Byte
33h	Reserved. Do not use
34h	Reserved. Do not use
35h	Low byte of extended memory (POST) in 64 KB
36h	High byte of extended memory (POST) in 64 KB
37h-3Dh	Varies
3Eh	Extended CMOS Checksum, Low Byte (including 34h-3Dh)
3Fh	Extended CMOS Checksum, High Byte (including 34h-3Dh)

I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses, which also becomes the identity of the device. There is a total of 1K-port address space available. The following table lists the I/O port addresses used on the Industrial CPU Card.

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	Timer
060h - 06Fh	Keyboard Controller
070h - 071h	Real Time Clock, NMI
080h - 09Fh	DMA Page Register
0A0h - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h	Clear Math Coprocessor Busy Signal
0F1h	Reset Math Coprocessor
1F0h - 1F7h	IDE Interface
2E8h - 2EFh	Serial Port #4(COM4)
2F8h - 2FFh	Serial Port #2(COM2)
2B0 - 2DF	Graphics adapter Controller
378h - 3FFh	Parallel Port #1(LPT1)
360 - 36F	Network Ports
3B0 - 3BF	Monochrome & Printer adapter
3C0 - 3CF	EGA adapter
3D0 - 3DF	CGA adapter
3E8h - 3EFh	Serial Port #3(COM3)
3F0h - 3F7h	Floppy Disk Controller
3F8h - 3FFh	Serial Port #1(COM1)

Interrupt Request Lines (IRQ)

There are a total of 15 IRQ lines available on the Industrial CPU Card. Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on the Industrial CPU Card.

Level	Function
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ2	Interrupt Cascade
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ5	Reserved
IRQ6	Floppy Disk Controller
IRQ7	Parallel Port #1
IRQ8	Real Time Clock
IRQ9	Reserved
IRQ10	Ethernet
IRQ11	Reserved
IRQ12	PS2-Mouse
IRQ13	FPU
IRQ14	Primary IDE
IRQ15	Reserved

DMA Channel Map

The equivalent of two 8237A DMA controllers are implemented in the VS-2510 board. Each controller is a four-channel DMA device that will generate the memory addresses and control signals necessary to transfer information directly between a peripheral device and memory. This allows high speed information transfer with less CPU intervention. The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 channel 0 provides the cascade interconnection between the two DMA devices, thereby maintaining IBM PC/AT compatibility.

The following is the system information of DMA channels:

DMA Controller 1	DMA Controller 2
Channel 0: Spare	Channel 4: Cascade for controller 1
Channel 1: Reserved for IBM SDLC	Channel 5: Spare
Channel 2: Diskette adapter	Channel 6: Spare
Channel 3: Spare	Channel 7: Spare

Serial Ports

The ACEs (Asynchronous Communication Elements ACE1 to ACE4) are used to convert parallel data to a serial format on the transmit side and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The ACEs are capable of handling divisors of 1 to 65535, and produce a 16x clock for driving the internal transmitter logic.

Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the ACE is a completed MODEM control capability, and a processor interrupt system that may be software tailored to the computing time required to handle the communications link.

The following table is a summary of each ACE accessible register

DLAB	Port Address	Register
0	Base + 0	Receiver buffer (read)
		Transmitter holding register (write)
0	Base + 1	Interrupt enable
X	Base + 2	Interrupt identification (read only)
X	Base + 3	Line control
X	Base + 4	MODEM control
X	Base + 5	Line status
X	Base + 6	MODEM status
X	Base + 7	Scratched register
1	Base + 0	Divisor latch (least significant byte)
1	Base + 1	Divisor latch (most significant byte)

❑ **Receiver Buffer Register (RBR)**

Bit 0-7: Received data byte (Read Only)

❑ **Transmitter Holding Register (THR)**

Bit 0-7: Transmitter holding data byte (Write Only)

❑ **Interrupt Enable Register (IER)**

Bit 0: Enable Received Data Available Interrupt (ERBFI)

Bit 1: Enable Transmitter Holding Empty Interrupt (ETBEI)

Bit 2: Enable Receiver Line Status Interrupt (ELSI)

Bit 3: Enable MODEM Status Interrupt (EDSSI)

Bit 4: Must be 0

Bit 5: Must be 0

Bit 6: Must be 0

Bit 7: Must be 0

□ **Interrupt Identification Register (IIR)**

Bit 0: "0" if Interrupt Pending

Bit 1: Interrupt ID Bit 0

Bit 2: Interrupt ID Bit 1

Bit 3: Must be 0

Bit 4: Must be 0

Bit 5: Must be 0

Bit 6: Must be 0

Bit 7: Must be 0

□ **Line Control Register (LCR)**

Bit 0: Word Length Select Bit 0 (WLS0)

Bit 1: Word Length Select Bit 1 (WLS1)

WLS1	WLS0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: Number of Stop Bit (STB)

Bit 3: Parity Enable (PEN)

Bit 4: Even Parity Select (EPS)

Bit 5: Stick Parity

Bit 6: Set Break

Bit 7: Divisor Latch Access Bit (DLAB)

□ **MODEM Control Register (MCR)**

Bit 0: Data Terminal Ready (DTR)

Bit 1: Request to Send (RTS)

Bit 2: Out 1 (OUT 1)

Bit 3: Out 2 (OUT 2)

Bit 4: Loop

Bit 5: Must be 0

Bit 6: Must be 0

Bit 7: Must be 0

□ **Line Status Register (LSR)**

Bit 0: Data Ready (DR)

Bit 1: Overrun Error (OR)

Bit 2: Parity Error (PE)

Bit 3: Framing Error (FE)

Bit 4: Break Interrupt (BI)

Bit 5: Transmitter Holding Register Empty (THRE)

Bit 6: Transmitter Shift Register Empty (TSRE)

Bit 7: Must be 0

□ **MODEM Status Register (MSR)**

Bit 0: Delta Clear to Send (DCTS)

Bit 1: Delta Data Set Ready (DDSR)

Bit 2: Training Edge Ring Indicator (TERI)

Bit 3: Delta Receive Line Signal Detect (DSLSD)

Bit 4: Clear to Send (CTS)

Bit 5: Data Set Ready (DSR)

Bit 6: Ring Indicator (RI)

Bit 7: Received Line Signal Detect (RSLD)

□ **Divisor Latch (LS, MS)**

	LS	MS
Bit 0:	Bit 0	Bit 8
Bit 1:	Bit 1	Bit 9
Bit 2:	Bit 2	Bit 10
Bit 3:	Bit 3	Bit 11
Bit 4:	Bit 4	Bit 12
Bit 5:	Bit 5	Bit 13
Bit 6:	Bit 6	Bit 14
Bit 7:	Bit 7	Bit 15

Desired Baud Rate	Divisor Used to Generate 16x Clock
300	384
600	192
1200	96
1800	64
2400	48
3600	32
4800	24
9600	12
14400	8
19200	6
28800	4
38400	3
57600	2
115200	1

Parallel Ports

□ Register Address

Port Address	Read/Write	Register
Base + 0	Write	Output data
Base + 0	Read	Input data
Base + 1	Read	Printer status buffer
Base + 2	Write	Printer control latch

□ Printer Interface Logic

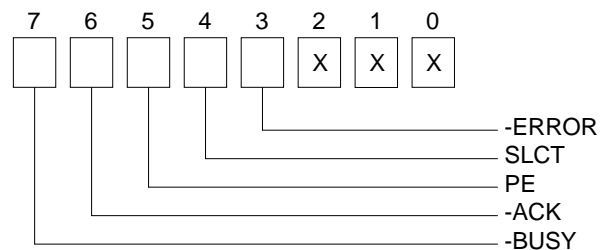
The parallel portion of the SMC37C669 makes the attachment of various devices that accept eight bits of parallel data at standard TTL level.

□ Data Swapper

The system microprocessor can read the contents of the printer's Data Latch through the Data Swapper by reading the Data Swapper address

□ Printer Status Buffer

The system microprocessor can read the printer status by reading the address of the Printer Status Buffer. The bit definitions are described below:

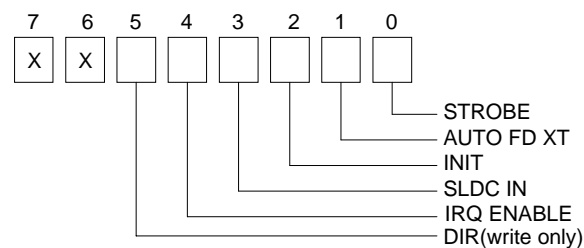


NOTE: X represents not used.

-
-
- Bit 7: This signal may become active during data entry, when the printer is off-line during printing, or when the print head is changing position or in an error state. When Bit 7 is active, the printer is busy and cannot accept data.
- Bit 6: This bit represents the current state of the printer's ACK signal. A 0 means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before receiving a BUSY message stops.
- Bit 5: A 1 means the printer has detected the end of the paper.
- Bit 4: A 1 means the printer is selected.
- Bit 3: A 0 means the printer has encountered an error condition.

□ **Printer Control Latch & Printer Control Swapper**

The system microprocessor can read the contents of the printer control latch by reading the address of printer control swapper. Bit definitions are as follows:



NOTE: X represents not used.

-
-
- Bit 5: Direction control bit. When logic 1, the output buffers in the parallel port are disabled allowing data driven from external sources to be read; when logic 0, they work as a printer port. This bit is write-only.
- Bit 4: A 1 in this position allows an interrupt to occur when ACK changes from low state to high state.
- Bit 3: A 1 in this bit position selects the printer.
- Bit 2: A 0 starts the printer (50 microseconds pulse, minimum).
- Bit 1: A 1 causes the printer to line-feed after a line is printed.
- Bit 0: A 0.5 microsecond minimum highly active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.